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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,189	05/25/2001	Ryoichi Matsumoto	OKI.237	2192

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EXAMINER	
LE, THIEN MINH	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,189	MATSUMOTO, RYOICHI	
	Examiner	Art Unit	
	Thien M. Le	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☒ Claim(s) 10-27 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 May 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The priority document filed on 7/6/2000 has been entered. Claims 1-27 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiguchi (Nishiguchi – 5,188,984).

Regarding claim 1, Nishiguchi discloses in figure 2c "a gallium arsenide chip 55 of approximately 180 .mu.m thick having an integrated circuit pattern (not shown) is disposed in the concave portion 54 so as to provide a die-bonding of approximately 20 .mu.m thick with eutectic crystal alloy of aurum and tin for example. Upon processing as mentioned above, the thickness of the gallium arsenide chip 55 and the die-bonding is equal to the depth of the concave portion 54, therefore, the level of the surface of the gallium arsenide chip 55 coincides with the level of the surface of the silicon substrate 51.

Further, according to Nishiguchi: "Subsequently, as shown in FIG. 2(d), an insulating film 56 made of such as polyimide is coated on the whole surface of the substrate 51 and the surface of the electrodes of the chips 55 then the coated insulating film 56 is patterned so that the electrodes on the gallium arsenide chips 55 and the circuit on the surface of the substrate 51 are exposed. In the case of the present embodiment, though the spaces between the surrounding wall 54a of the concave portion 54 and the side wall of the gallium arsenide chip 55 are not usually filled with filler perfectly, since the space are so minute that it is not necessary to fill the spaces perfectly, but the spaces may be also filled perfectly.

Next, there is formed a thin film conducting layer on the whole surface of the insulating film 56 by sputtering aluminum, for example, subsequently the conducting layer is patterned for forming an upper thin film connecting circuit layer 57 for connecting the electrodes on the gallium arsenide chip 55 and the first connecting circuit pattern 60 previously formed on the surface of the substrate 51. The width of the upper thin film connecting circuit pattern 57

is approximately 10 .mu.m, which is wider than that of a usual thin film circuit, and since there does not occur such a deformation such as occurs in a wire arrangement in the conventional semiconductor device, it is possible to make a thin film circuit having a higher circuit pattern density than that of the conventional device. " (see the descriptions of figures 2a-2e).

As can be seen, Nishiguchi discloses a method of manufacturing a semiconductor device comprising the step of forming an insulating layer 56 on the chip 55; forming a conductive layer 57 on top of the insulating layer 56; and the method of implanting the conducting layer by sputtering aluminum. Thus, Nishiguchi discloses the claimed invention.

Regarding claim 8, Nishiguchi discloses that the conducting layer is made of Alumium and thus would embrace all limitations set forth in this claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi (Nishiguchi – 5,188,984) in view of Shimada (Shimada – 6,002,383).

Regarding claim 2, see the discussions regarding claim 1. The claim differs in calling for a conductive layer which is made of carbon. However, the use of carbon as conductive material in semiconductor device is not new.

Reference to Shimada is cited as an evidence showing the conventionality of the this claimed limitation. Specifically, Shimada discloses a conductive layer 26 which contains carbon material. (see figure 12)

It would have been obvious to implement the use of a conductive layer that is made of carbon in the system and method as taught by Nishiguchi. The modification merely replaces one type of conductive layer with another type of conductive layer and thus is viewed as substitution of art recognized equivalent that is well within the skill levels and expectations of an ordinary skilled artisan.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi (Nishiguchi – 5,188,984) in view of Shimada (Shimada – 6,002,383) and further in view of Tsutsumi (Tsutsumi – 5,789,792).

Regarding claim 3, see the discussions regarding claims 1 and 2. The claim differs in calling the specific range of thickness for the conductive layer.

However, this claimed limitation is not new.

Reference to Tsutsumi is cited as an evidence showing the conventionality of the method of forming a conductive layer having thickness of 7nm – 700 nm (see descriptions of figure 10).

It would have been obvious to implement a conductive layer having the thickness as taught by Tsutsumi in the system and method as taught by Nishiguchi/Shimada. The modification is merely a substitution of one conductive layer with another conductive layer having a specific thickness.

Regarding claim 4, see the discussions regarding claim 1. The claim differs in calling for the conductive layer which is made of silicon doped with impurity ions. Reference to Tsutsumi also discloses the missing limitation. Speficially, Tsutsumi discloses that "Referring to FIG. 10, a thermal oxidation method or a CVD method is performed to from silicon oxide film 5 of 5 nm in thickness on the main surface of semiconductor substrate 1 at the transistor formation region. Thereafter, a CVD method is performed to form conductive layer 7 of 700 nm in thickness made of, e.g., a polycrystalline silicon film doped with impurity. (see the descriptions of figure 10)

It would have been obvious to incorporate implement the conductive layer which is made of silicon and impurity ions in the manner in the combined system and method of Nishiguchi/Shimada. The modification merely replaces one type of conductive layer with another type of conductive layer and thus is viewed as substitution of art recognized equivalent that is well within the skill levels and expectations of an ordinary skilled artisan.

Regarding claim 5, see the discussions regarding claims 3-4.

Claims 6-7, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi (Nishiguchi – 5,188,984) in view of Hara et al. (Hara et al. – herein after referred to as Hara – 5,946,167).

Regarding claims 6-7, 9, see the discussions regarding claims 1-5. The claims differ in calling for the conductive layer which is made of a metal group including gold (Au), an Au-alloy, Platinum (Pt), Al-alloy, etc. However, these claimed limitations are not new.

Reference to Hara is cited as an evidence showing the conventionality of the claimed limitation. Specifically, Hara discloses that "conductive layer may comprise Cu, Au, Ag, Pt, Pd, Ru, Rh, Ir, a CuPd alloy, a CuAu alloy or CuPt alloy. The thickness of the nonmagnetic conductive layer may be between about 0.5 nm and about 20 nm. " (see col. 4-5)

It would have been obvious to implement the use of a conductive layer that is made of Au, Pt, etc., in the system and method as taught by Nishiguchi. The modification merely replaces one type of conductive layer with another type of conductive layer and thus is viewed as substitution of art recognized equivalent that is well within the skill levels and expectations of an ordinary skilled artisan.

Allowable Subject Matter

Claims 10-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a method as recited in claim 1, further comprising the step of forming a second insulating layer having an active region in the manner as recited in claims 10-27.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien M. Le whose telephone number is (571) 272-2396. The examiner can normally be reached on Monday - Friday from 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Le, Thien Minh
Primary Examiner

Art Unit 2876
September 14, 2005